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December 24, 1997

Attorney Docket No.: 06802/148001

## Box Patent Application

Assistant Commissioner for Patents

Washington, DC 20231

Presented for filing is a new original patent application of:

Applicant: IM CHEOL HA  
Title: DECODER CIRCUIT IN A FLASH MEMORY DEVICE

Enclosed are the following papers, including all those required to receive a filing date under 37 CFR §1.53(b):

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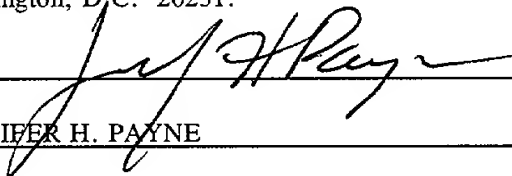
### Enclosures:

- Rule 63 declaration, copy from a previous application under rule 63(d) for continuation or divisional only.
- New disclosure information, including:
  - Information disclosure statement, 2 pages.
  - PTO-1449, 1 pages.
  - References, 1 items.
- Certified copies of priority document(s) no(s) 96-74959 and 96-74963.
- Postcard.

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BOX PATENT APPLICATION

December 24, 1997

Page 2

Under 35 USC §119, this application claims the benefit of foreign priority applications filed in Korea, serial number 96-74959, filed December 28, 1996, and serial number 96-74963, filed December 28, 1996.

Basic filing fee	\$ 0.00
Total claims in excess of 20 times \$22.00	0.00
Independent claims in excess of 3 times \$82.00	0.00
Multiple dependent claims	0.00
Total filing fee:	\$ 0.00

Under 37 CFR §1.53(d), no filing fee is being paid at this time. Please apply any other required fees, **EXCEPT FOR THE FILING FEE**, to deposit account 06-1050, referencing the attorney docket number shown above. A duplicate copy of this transmittal letter is attached.


If this application is found to be INCOMPLETE, or if a telephone conference would otherwise be helpful, please call the undersigned at 619/678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

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Respectfully submitted,

  
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Enclosures

48600.LJ1

06990157-122497

APPLICATION  
FOR  
UNITED STATES LETTERS PATENT

TITLE: DECODER CIRCUIT IN A FLASH MEMORY DEVICE

APPLICANT: IM CHEOL HA

08998157 122497

"EXPRESS MAIL" Mailing Label Number EM153707102US

Date of Deposit DECEMBER 24, 1997

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JENNIFER H. PAYNE



## DECODER CIRCUIT IN A FLASH MEMORY DEVICE

### BACKGROUND OF THE INVENTION

#### Field of the Invention

The present invention relates to a row decoder circuit in a flash memory device which can increase the number of a local row decoder, to which an output of a global row decoder is input, as many number of sectors when the sectors are divide in a column direction.

#### Description of the Prior Art

Generally, a flash memory device has both functions of electrical program and erasure. In the flash memory device capable of programming sector-by-sector, it is a general requirement that the write cycle of more than a hundred thousand has to be guaranteed. At this time, the number of stress acted to the gate of unit cell is same as the number of the unit cell connected to a single word line, and the number of stress acted to the drain of unit cell is same as the number of the unit cell connected to a single bit line.

FIG. 1 is a circuit diagram of a conventional row decoder.

In a read mode, a first voltage supply signal **SnVppx** of a selected sector is switched to a Vdd voltage level and a second voltage supply signals **SnVeex** and **XRST** thereof are switched to a ground voltage level. At this time, as a

PMOS transistor **hp1** is turned on, a node **A** has a Vdd voltage level and the Vdd voltage level of the node **A** turns on a NMOS transistor **thn**, thus a sector word line signal **SnWL** maintains a ground voltage level.

On the other hand, one **XnCOM** selected by a NAND gate I to which row address signals **XPRED** and **XCPRED** and a sector signal **S** are input maintains a ground voltage level. At this time, since only a single **XAPRED** maintains a Vdd voltage level, a NMOS transistor **hn** of the row decoder which will be selected is turned on, the node **A** of the selected row decoder maintains a ground voltage level. Therefore, the ground voltage level applied to the node **A** causes a PMOS transistor **hp3** to turn on, thus a sector word line signal **SnWL** maintains a Vpp voltage level.

In a program mode, the first voltage supply signal **SnVppx** of the selected sector is switched to a Vpp voltage level, the second voltage supply signal **SnVeex** thereof is switched to a ground voltage level. The **XRST** thereof maintains a ground voltage level before the first voltage supply signal **SnVppx** is switched to Vpp voltage and is switched to Vpp voltage level when the first voltage supply signal **SnVppx** is switched to Vpp voltage. A first voltage supply signal **SnVppx** of a non-selected sector maintains a Vdd voltage level and the **XRST** of the non-selected sector maintains a ground voltage level so that a word line **SnWL** of the not-selected sector is switched to a ground voltage level.

On the other hand, one **XnCOM** selected by a NAND gate I to which row address signals **XPRED** and **XCPRED** and the sector signal **S** are input maintains a ground voltage level. At this time, since only a single **XAPRED** maintains a  $V_{dd}$  voltage level, a NMOS transistor **hn** of the row decoder which will be selected is turned on, the node **A** of the selected row decoder maintains a ground voltage level. Therefore, the ground voltage level applied to the node **A** causes a PMOS transistor **hp3** to turn on, thus a sector word line signal **SnWL** maintains a  $V_{pp}$  voltage level.

In an erase mode, the first voltage supply signal **SnVppx** of the selected sector is switched to a ground voltage level, the second voltage supply signal **SnVeex** thereof is switched to a  $-V_{pp}$  voltage level, and **XRST** thereof is switched to a ground voltage level. And, a first voltage supply signal **SnVppx** of a non-selected sector is switched to a  $V_{dd}$  voltage level, a second voltage supply signal **SnVeex** thereof is switched to a ground voltage level, and the **XRST** thereof is switched to a ground voltage level.

As a result, as the node **A** of the non-selected sector is at  $V_{dd}$  voltage level, the sector word line thereof maintains a ground voltage level. Meanwhile, as the NMOS transistor **thn** in the row decoder of the selected sector is turned on, all the word line signals **SnWL** maintain a  $-V_{pp}$  voltage level.

In the row decoder as described above, the number of the row decoder is increased as many when the sector is divided in a column direction, the number

of **XnCOM** of the row decoder is increased. Therefore, a free decoder output load and an address buffer output load are increased proportionally. As a result, an access time is delayed and the size of a chip becomes large.

## SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a row decoder circuit which can minimize a load due to a row address signal and decrease an access time and a size of chip due to the local row decoder having a simply circuit.

A decoder circuit according to the present invention comprises a global row decoder consisted of a first decoding means selected according to a row address signal and a second decoding means to which an output signal of the first decoding means and an erasure signal are input and a local row decoder for selecting each global word line signal outputted from the global row decoder.

The local row decoder is consisted of a first and second transistors to the word line signal is input, and a third, fourth and fifth transistors outputting a first voltage supply signal and a second voltage supply signal to a sector word line

Another decoder circuit of the present invention comprises a global row decoder for outputting a global word line signal and a local row decoder for selecting a word line in response to the global word line signal of the global

row decoder. The global row decoder is consisted of a first and second transistors to which XnCOM signal is input and a third and fourth transistors, to which an output voltage of the first and second transistors, for outputting a Vppx or Veex to a global sector word line.

### **Brief description of the drawings**

Other objects and advantages of the present invention will be understood by reading the detailed explanation of the embodiment with reference to the accompanying drawings in which:

FIG. 1 is a circuit diagram illustrating a conventional row decoder.

FIG. 2 is a circuit diagram illustrating a global row decoder according to the first embodiment of the present invention.

FIG. 3 is a circuit diagram illustrating a local row decoder according to the first embodiment of the present invention.

FIG. 4 is a circuit diagram illustrating a global row decoder according to the second embodiment of the present invention.

FIG. 5 is a circuit diagram illustrating a local row decoder according to the second embodiment of the present invention.

### **Detailed description of the drawings**

Below, the preferred embodiments of the present invention will be in



detail explained by reference to the accompanying drawings.

FIG. 2 is a circuit diagram illustrating a global row decoder according to the first embodiment of the present invention.

An output signal of a first decoding means **I11** is determined by row address signals **XAPRED**, **XPRED** and **XCPRED**. The output signal of the first decoding means **I11** and an erasure signal **E** are input to a second decoding means **I12**, thereby outputting a global word line signal **GWL**. The first and second decoding means **I11** and **I12** are consisted of NAND gates. That is, in a read mode and a program mode, only one of a plurality of global word line signals **GWL** is selected as a Vdd voltage level. In erasure mode, since the erasure signal **E** maintains a ground voltage level, the global word line signal **GWL** in all the global row decoder maintains a Vdd voltage level.

FIG. 3 is a circuit diagram of a local row decoder. The global word line signal **GWL** is input to the local row decoder, the global word line signal **GWL** transfers to a sector word line of the column sector selected by means of the combination of the column sector address **SnCOM**. Also, a sector word line signal **SnWL** of a non-selected column sectors maintains a ground voltage level.

The operations of the local row decoder will be explained mode-by-mode as follows.

In a read mode, a first voltage supply signal **SnVppx** of all the column sectors is switched to a Vdd voltage level and a second voltage supply signal

SnVeex thereof is switched to a ground voltage level. The selected column sector address signal **SnCOM** of the column sector is switched to a ground voltage level and the non-selected column sector address signal **SnCOM** of the column sector is switched to a Vdd voltage level. As a result, as a second transistor **T2** of the local row decoder is turned on by the non-selected global word line signal **GWL**, a voltage of the node **B** maintains a Vdd voltage level, and the voltage of the node **B** turns on a fifth transistor **T5**, thus the sector word line signal **SnWL** maintains a ground voltage level.

On the other hand, the selected global word line signal **GWL** becomes a Vdd voltage level so that the first transistor **T1** is turned on, thus a voltage of the node **B** becomes a voltage of the column sector address signal **SnCOM** by means of the column sector. Therefore, since the column sector address signal **SnCOM** of the non-selected column sectors is at Vdd voltage level, the fifth transistor **T5** is turned on. Thus, the sector word line signal **SnWL** becomes a ground voltage level. Since the only column sector address signal **SnCOM** of the selected column sectors becomes a ground voltage level, the fourth transistor **T4** is turned on and the sector word line signal **SnWL** has a Vdd voltage level. As a result, only one selected sector word line signal **SnWL** of all the sector word lines **SnWL** has a Vdd voltage level, and the other sector word line signals **SnWL** maintain a ground voltage level.

Next, in a program mode, the first voltage supply signal **SnVppx** of a

selected sector is switched to a  $V_{pp}$  voltage level, the first voltage supply signal  $S_nV_{ppx}$  of non-selected sectors is switched to a  $V_{dd}$  voltage level, and all second voltage supply signals  **$S_nVeex$**  are switched to a ground voltage level. Also, the column sector address signal  **$S_nCOM$**  of the selected column sector is switched to a ground voltage level and the non-selected column sector address signal  **$S_nCOM$**  is switched to a  $V_{dd}$  voltage level. Therefore, the non-selected global word line signal  **$GWL$**  turns on the second transistor  **$T2$**  so as to switch a voltage of the node  **$B$**  to a  $V_{dd}$  voltage level and the  $V_{dd}$  voltage level applied to the node  **$B$**  turns on the fifth transistor  **$T5$** . Therefore, a corresponding sector word line signal  **$S_nWL$**  maintains a ground voltage level.

Meanwhile, the selected global word line signal  **$GWL$**  turns on the first transistor  **$T1$** , therefore, the node  **$B$**  maintains a voltage of a column sector address signal  **$S_nCOM$**  by means of a column sector. At this time, the third and the fifth transistors  **$T3$**  and  **$T5$**  in the non-selected column sector are turned on, therefore, the sector word line signal  **$S_nWL$**  maintains a ground voltage level. And, the fourth transistor  **$T4$**  in the selected column sector is turned on, therefore, the sector word line signal  **$S_nWL$**  maintains a  $V_{pp}$  voltage level.

As a result, only one selected sector word line signal  **$S_nWL$**  of all the sector word lines signal  **$S_nWL$**  has a  $V_{pp}$  voltage level, and the other sector word line signals  **$S_nWL$**  maintains a ground voltage level.

In an erasure mode, the first voltage supply signal  **$S_nV_{ppx}$**  of a selected

sector is switched to a ground voltage level and the second voltage supply signal  $\text{SnVeex}$  is switched to a  $-V_{pp}$  voltage level. And, the first voltage supply signals  $\text{SnVppx}$  of non-selected sectors are switched to a  $V_{dd}$  voltage level and the second voltage supply signals  $\text{SnVeex}$  of the non-selected sectors are switched to a ground voltage level. Since a voltage of the global word line signal  $\text{GWL}$  which is an output signal of the global low decoder is at  $V_{dd}$  voltage level, the first transistor  $\text{T1}$  is turned on by means of the global word line signal  $\text{GWL}$ , thus the node  $\text{B}$  maintains a voltage of a column sector address signal  $\text{SnCOM}$  by means of the column sector. At this time, as the first voltage supply signal  $\text{SnVppx}$  and the column sector address signal  $\text{SnCOM}$  of the non-selected sectors maintain  $V_{dd}$  voltage level, the node  $\text{B}$  maintains a  $V_{dd}$  voltage level and the fifth transistor  $\text{T5}$  is turned on. As a result, the sector word line signal  $\text{SnWL}$  of the non-selected sectors maintain a ground voltage level.

On the other hand, since the first voltage supply signal  $\text{SnVppx}$  of a selected sector maintains a ground voltage level, the second voltage supply signal  $\text{SnVeex}$  is at  $-V_{pp}$  voltage level and the column sector address signal  $\text{SnCOM}$  maintain a ground voltage level, the fifth transistor  $\text{T5}$  of all the local row decoders of the selected sector is turned on and all the sector word line signals  $\text{SnWL}$  of the selected sector maintain a  $-V_{pp}$  voltage level.

FIG. 4 is a circuit diagram illustrating a global row decoder according to

the second embodiment of the present invention. **XnCOM** of a global row decoder selected by a row address signal maintains a Vdd voltage level.

Explanation for the operations will be given mode-by-mode as follow.

In a read mode, **Vppx** is switched to a Vdd voltage level and **Veex** is switched to a ground voltage level. At this time, as **XnCOM** of a selected global row decoder is at Vdd voltage level, a second transistor **T12** is turned off and a first transistor **T11** is turned on. Therefore, the node **B** maintains a ground voltage level so that the fourth transistor **T14** is turned on and the global word line signal **GWL** maintains a Vdd voltage level.

Meanwhile, as **XnCOM** of a non-selected global row decoder maintains a ground voltage level, the second transistor **T12** is turned on, thus the node **B** maintains a Vdd voltage level. Therefore, a third transistor **T13** is turned on so that non-selected global word line signal **GWL** maintains a ground voltage level.

In a program mode, **Vppx** of the global row decoder is switched to a Vpp voltage level by means of a selected row sector address, and **Vppx** of non-selected global row decoders is switched to a Vdd voltage level. At this time, the first transistor **T11** of the selected global row decoder is turned on so that the node **B** maintains a ground voltage level. As a result, the fourth transistor **T14** is turned on and thus the selected global word line signal **GWL** maintain a Vpp voltage level.

Meanwhile, as **XnCOM** of the non-selected global row decoder maintains

a ground voltage level, the second transistor **T12** is turned on so that the node **B** maintains a  $V_{pp}$  voltage level, Also, the third transistor **T13** is turned on so that the non-selected global word line signal **GWL** maintains a ground voltage level.

Finally, in an erasure mode,  $V_{ppx}$  of the global row decoder selected by a row sector address is switched to a ground voltage level and  $V_{ppx}$  of the non-selected global row decoders is switched to a  $V_{dd}$  voltage level. And,  $V_{eex}$  of the selected global row decoder is switched to a  $-V_{pp}$  voltage level and  $V_{ppx}$  of the non-selected global row decoders is switched to a ground voltage level. Also, as **XnCOM** of the global row decoder maintains a  $V_{dd}$  voltage level by an erase signal in the erasure mode and  $V_{eex}$  of the row sector selected by the row sector address is at  $-V_{pp}$  voltage level, the first and the third transistors **T11** and **T13** in the global row decoder of the selected row sector are turned on and thus the all global word line signal **GWL** maintain a  $-V_{pp}$  voltage level.

Meanwhile,  $V_{eex}$  of the non-selected global row decoder maintains a ground voltage level and  $V_{ppx}$  thereof maintains a  $V_{dd}$  voltage level so that the second and the third transistors **T12** and **T13** are turned on, thus the global word line signal **GWL** maintains a ground voltage level.

FIG. 5 is a circuit diagram of a local row decoder. In the local decoder to which the global word line signal **GWL** is input, the voltage level of the

global word line signal **GWL** is transferred to the only column sector selected by a combination of the first and the second column sector address signals **SnCOM** and **SnCOMB**, and the word line signal **GWL** of the non-selected column sectors maintains a ground voltage level.

**Vppx** and **Veex** of the local row decoder and **Vppx** and **Veex** of the global row decoder are switched according to the each mode. And, although the fifth transistor **T15** and the sixth transistor **T16** in the local row decoder of a column sector selected by a combination of a gate input of the local row decoder (the first and the second column sector address signals **SnCOM** and **SnCOMB**), **Vppx** and **Veex** are turned on, the fifth transistor **T15** and the sixth transistor **T16** in the local row decoder of non-selected column sector are turned off and the seventh transistor **T17** is turned on so that the word line signal **SnWL** maintains a ground voltage level.

Explanation of the operation will be described mode-by-mode.

In a read mode, **Vppx** maintains a **Vdd** voltage level and **Veex** maintains a ground voltage level. A selected global word line **GWL** maintains a **Vdd** voltage level and a non-selected global word line signal **GWL** maintains a ground voltage level. At this time, as a first column sector address **SnCOM** is switched to a ground voltage level and a second column sector address **SnCOMB** is switched to a **Vdd** voltage level, the fifth and the sixth transistors **T15** and **T16** of a selected column sector are turned on, and the seventh

transistor **T17** is turned off, so that the word line signal **SnWL** maintains a Vdd voltage level of the global word line signal **GWL**.

Meanwhile, as the first column sector address signal **SnCOM** is switched to a Vdd voltage level and the second column sector address signal **SnCOMB** is switched to a Vdd voltage level, the fifth and the sixth transistor **T15** and **T16** of a non-selected column are turned off and the seventh transistor **T17** is turned on so that the word line signals **SnWL** maintain a ground voltage level.

In a program mode, a selected global word line signal **GWL** maintains a Vpp voltage level and **Vppx** maintains a Vpp voltage level. And, a selected global word line signal **GWL** maintains a ground voltage level, **Vppx** maintains a Vdd voltage level, and **Veex** maintain a ground voltage level. As the first column sector address signal **SnCOM** maintains a Vdd voltage level and the second column sector address signal **SnCOMB** maintains a ground voltage level, the fifth and the sixth transistor **T15** and **T16** of the local row decoder in non-selected row sector are turned off and the seventh transistor **T17** is turned on so that the word line signal **SnWL** maintains a ground voltage level.

On the other hand, if the first column sector address signal **SnCOM** maintains a ground voltage level and the second column sector address signal **SnCOMB** maintains a Vdd voltage level, the fifth and the sixth transistor **T15** and **T16** of the local row decoder are turned on and the seventh transistor **T17** is turned off so that the global word line signal **GWL** maintains a voltage level



of the global the word line signal **SnWL**. As a result, only single word line signal **SnWL** maintains a  $V_{pp}$  voltage level and the other the word line signals **SnWL** maintain a ground voltage level.

In an erase mode, the global word line signal **GWL** selected by a row sector address maintains a  $-V_{pp}$  voltage level, **Vppx** maintains a ground voltage level and **Veex** maintains a  $-V_{pp}$  voltage level. And, a non-selected global word line signal **GWL** maintains a  $V_{dd}$  voltage level, **Vppx** maintains a  $V_{dd}$  voltage level, and **Veex** maintains a ground voltage level. Since the first column sector address signal **SnCOM** of the non-selected row sector maintains a  $V_{dd}$  voltage level and the second column sector address signal **SnCOMB** maintains a ground voltage level, the fifth and the sixth transistor **T15** and **T16** are turned off and the seventh transistor **T17** is turned on so that the word line signal **SnWL** of all the local row decoders maintain a ground voltage level.

The first column sector address signal **SnCOM** of a selected column sectors among the selected row sectors maintains a  $-V_{pp}$  voltage level and the second column sector address signal **SnCOMB** maintains a ground voltage level. And, the first column sector address signal **SnCOM** of the non-selected column sectors maintains a ground voltage level and the second column sector address signal **SnCOMB** maintains a  $-V_{pp}$  voltage level.

As a result, even though the global word line signal **GWL** maintains a  $-V_{pp}$  voltage level by means of the row sector address, the fifth and the sixth

transistors **T15** and **T16** of the local row decoders of the selected column sector are turned on and the seventh transistor **T17** is turned off so that the word line signal **SnWL** maintains a voltage level of the global word line **GWL**. Also, the fifth and the sixth transistors **T15** and **T16** of the local row decoders of the non-selected column sector are turned off and the seventh transistor **T17** is turned on so that the word line signal **SnWL** of the local row decoders of the non-selected column sector maintains a ground voltage level.

In the present invention as described above, a load due to a row address signal can be minimized by increasing a local row decoder to which an output of a global row decoder is input as many as a number of sector when the sector is divided in column direction, therefore, it is possible to decrease an access time and decrease a size of chip due to the local row decoder having a simply circuit. Also, it is possible to decrease a load to pumping voltage ( $V_{pp}$  and  $-V_{pp}$ )

The foregoing description, although described in its preferred embodiments with a certain degree of particularity, is only illustrative of the principle of the present invention. It is to be understood that the present invention is not to be limited to the preferred embodiments disclosed and illustrated herein. Accordingly, all expedient variations that may be made within the scope and spirit of the present invention are to be encompassed as further embodiments of the present invention.

**What is claimed is:**

1. A decoder circuit in a flash memory device comprising;  
  
a global row decoder for outputting a global word line signal, said global row decoder consisted of a first decoding means selected according to a row address signal and a second decoding means to which an output signal of said first decoding means and an erasure signal are input; and  
  
a local row decoder for selecting each global word line signal outputted from the said global row decoder.
2. The decoder circuit of claim 1, wherein said first and second decoding means are consisted of NAND gates.
3. The decoder circuit of claim 1, wherein said local row decoder is consisted of;  
  
a first and second transistors to said word line signal is input;  
  
and a third, fourth and fifth transistors outputting a first voltage supply signal and a second voltage supply signal to a sector word line.
4. The decoder circuit claim 3, wherein said second, third and fourth transistors are consisted of PMOS transistor, and said first and fifth transistors are consisted of NMOS transistor.

5. A decoder circuit in a flash memory device, comprising:  
a global row decoder for outputting a global word line signal; and  
a local row decoder for selecting a word line in response to said global word line signal of said global row decoder.

6. The decoder circuit of claim 5, wherein said global row decoder is consisted of;

a first and second transistors to which XnCOM signal is input, and  
a third and fourth transistors, to which an output voltage of said first and second transistors, for outputting a Vppx or Veex to a global sector word line.

7. The decoder circuit claim 6, wherein said first and third transistors are consisted of PMOS transistor, and said second and fifth transistors are consisted of NMOS transistor.

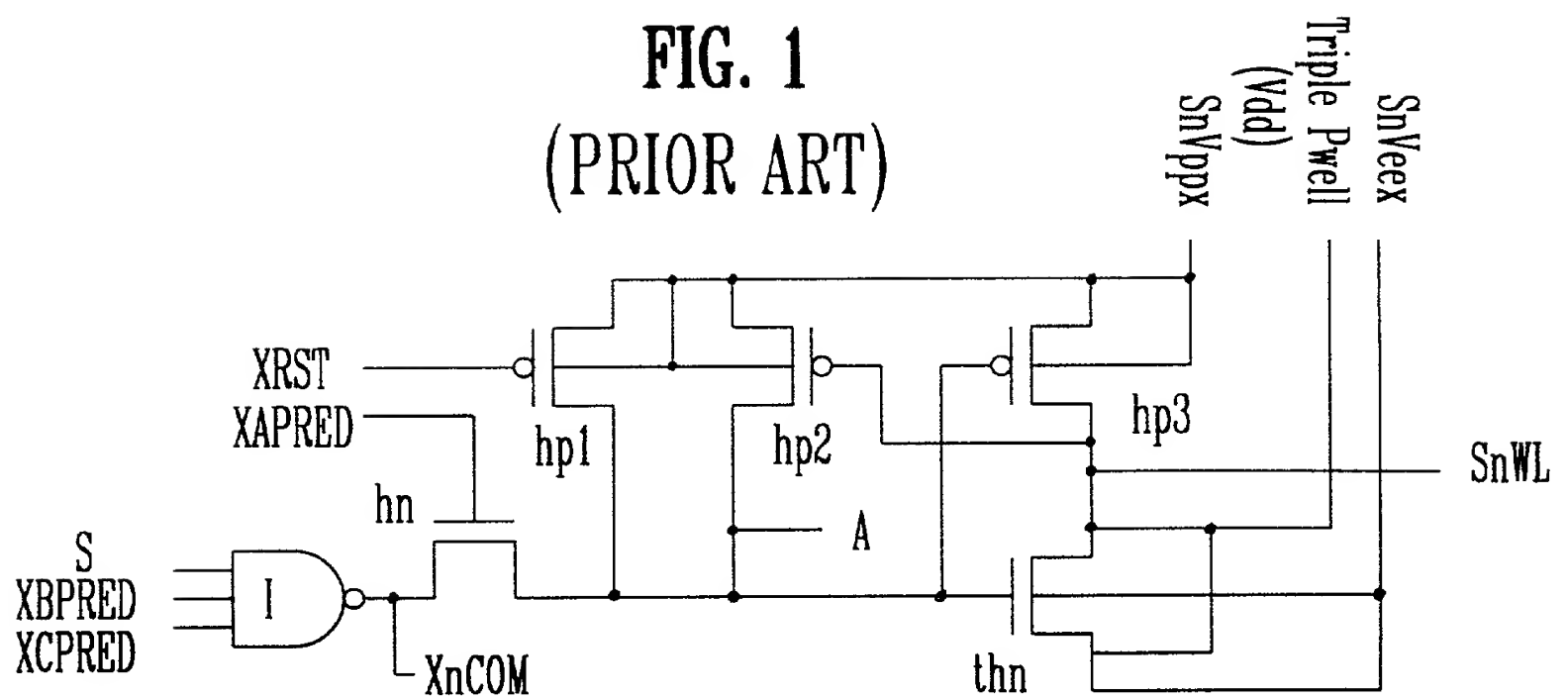
8. The decoder circuit of claim 5, wherein said local row decoder is consisted of a fifth, sixth and seventh transistor, to which said global word line is input, first and second transistors, for outputting said global word line to said word line.

9. The decoder circuit claim 8, wherein said fifth transistor is consisted of

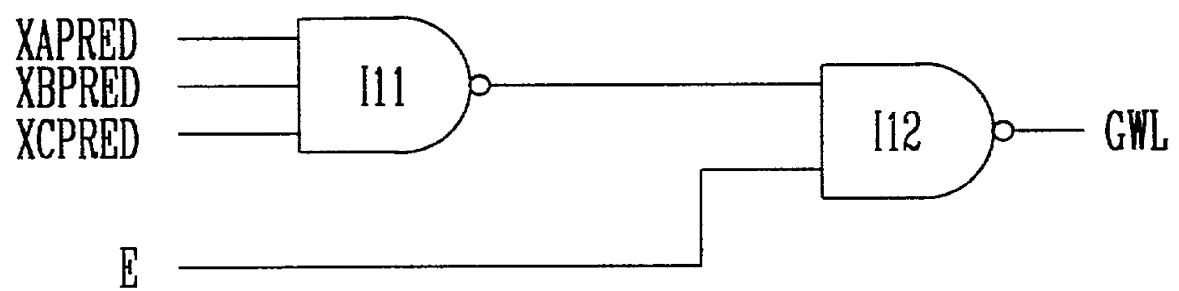
PMOS transistor, and said sixth and seventh transistors are consisted of NMOS transistor.



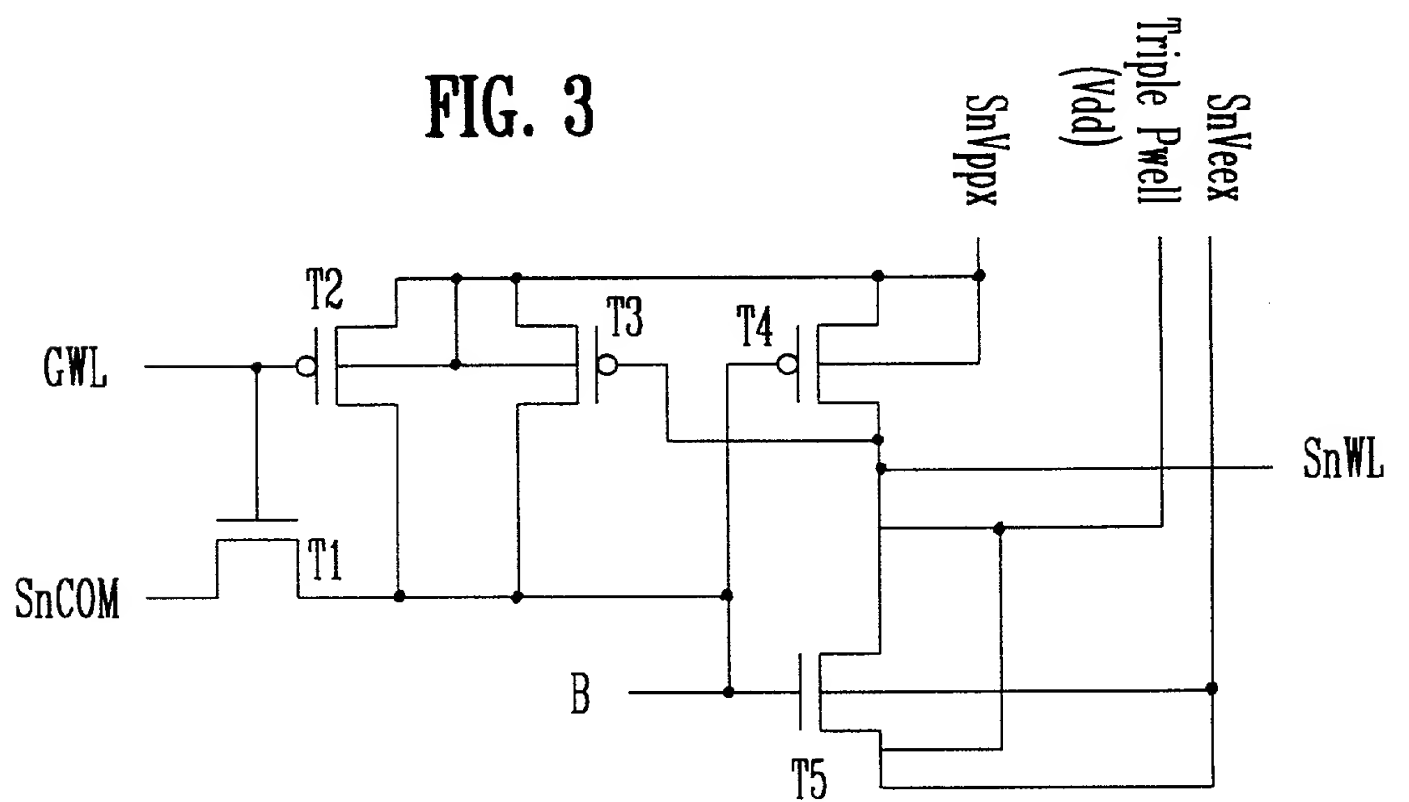
**FIG. 1**  
(PRIOR ART)

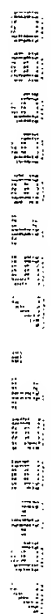
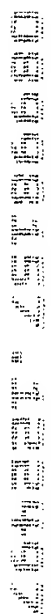


**FIG. 2**



**FIG. 3**



[illegible][illegible]



## PATENT

ATTORNEY DOCKET NO : 06802/148001

## COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **DECODER CIRCUIT IN A FLASH MEMORY DEVICE**, the specification of which

☒ is attached hereto.

☐ was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_\_ and was amended on \_\_\_\_\_.

☐ was described and claimed in PCT International Application No. \_\_\_\_\_ filed on \_\_\_\_\_ and as amended under PCT Article 19 on \_\_\_\_\_.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

COUNTRY	APPLICATION NO.	FILING DATE	PRIORITY CLAIMED
<u>Korea</u>	<u>96-74959</u>	<u>December 28, 1996</u>	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
<u>Korea</u>	<u>96-74963</u>	<u>December 28, 1996</u>	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
_____	_____	_____	<input type="checkbox"/> Yes <input type="checkbox"/> No

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Scott C. Harris, Reg. No. 32,030, William E. Booth, Reg. No. 28,933; John W. Freeman, Reg. No. 29,066; Timothy A. French, Reg. No. 30,175; Alan H. Gordon, Reg. No. 26,168; John F. Land, Reg. No. 29,544; John B. Pegram, Reg. No. 25,198; Rene D. Tegtmeyer, Reg. No. 33,567, Hans R. Troesch, Reg. No. 36,950; Dorothy P. Whelan, Reg. No. 33,814; Charles C. Wincheser, Reg. No. 21,040; John R. Wetherell, Jr., Reg. No. 31,678.

06802/148001

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any issued thereon.

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